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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,347	SORG ET AL.	
	Examiner	Art Unit	
	THANH Y. TRAN	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 6-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Shigeta et al (U.S. 6,107,678).

As to claim 1, Shigeta et al discloses in figures 10E-10H a surface-mountable miniature luminescent diode or photodiode comprising:

a chip package which has a leadframe (113/"patterns" 105); and a semiconductor chip (see the chip having connection terminals 110) which is arranged on, and is in electrical contact with, the leadframe (113/"patterns" 105) and which comprises a first contact area (first 105), a second contact area (second 105), and at least one of an active; wherein the leadframe (113/"patterns" 105) is formed by a flexible multi-layered sheet (comprising layers 106 & 105) comprising: a metal foil comprising a first chip connection region (a first chip connection region is a connection region of first terminal 110 on lead 105) and a second chip connection region (a second chip connection region is a connection region of second terminal 110 on lead 105), the first contact area (first terminal 110) of the semiconductor chip being disposed on the first chip connection region and the second contact area (second terminal 110) of the semiconductor chip being coupled to the second chip connection region; and a plastic film (106), arranged on, and connected to, the metal foil ("patterns" 105), the plastic film (106) defining a plurality of

openings in regions arranged on the first and the second chip connection regions (see figures 10E-10H, layer 106 having openings); and wherein the semiconductor chip (see the chip having terminals 110) is mounted in one of the plurality of openings of the plastic film (106) with the first contact area (first terminal 110) contacting the first chip connection region.

As to claim 3, Shigeta et al discloses in figures 10E-10H a surface-mountable miniature luminescent diode or photodiode with a chip package, wherein the plastic film (106) is adhesively bonded to the metal foil ("patterns" 105).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 6-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta et al (U.S. 6,107,678).

As to claims 6, 8 and 10-11, Shigeta et al does not disclose thickness of the metal foil is less than 80 μm; wherein the thickness of the plastic film is less than 80 μm; wherein the leadframe has footprint dimensions of approximately 0.5 mm x 1.0 mm or less; the luminescent diode has a total thickness of approximately 400 μm or less. However, *the dimension range for a metal foil or a leadframe; and a desired thickness range for a plastic film or a luminescent diode* would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 7, Shigeta et al does not disclose the plastic film comprises an epoxy resin film. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify apparatus of Shigeta et alby using epoxy resin film for forming a plastic film for providing a reliable thermally insulating layer for the semiconductor package, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

5. Claims 9, 12 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta et al (U.S. 6,107,678) in view of Galli et al (U.S. 3,781,596).

As to claims 9, 16 and 18, Shigeta et al does not disclose the semiconductor chip is embedded in an encapsulating material; wherein the encapsulating material is injection-molded onto the plastic film of the multi-layered sheet; and wherein the first and second chip connection regions of the leadframe are short-circuited and grounded in the steps of mounting the semiconductor chip, connecting the second contact area and encapsulating the semiconductor chip.

Galli et al discloses in figure 6b a semiconductor chip (30) is embedded in an encapsulating material (45); wherein the encapsulating material (45) is injection-molded onto the plastic film (10) of the multi-layered sheet (comprising elements 10, 42); and wherein the first and second chip connection regions (first and second chip connection regions are regions of 12 corresponding first and second "pads" 31) of the leadframe (comprising elements 10, 42) are short-circuited and grounded in the steps of mounting the semiconductor chip (30), connecting the second contact area (second "pad" 31) and encapsulating the semiconductor chip (30). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Shigeta et al by having a semiconductor chip that is embedded in an encapsulating material; wherein the encapsulating material is injection-molded onto the plastic film of the multi-layered sheet; and wherein the first and second chip connection regions of the leadframe are short-circuited and grounded in the steps of mounting the semiconductor chip, connecting the second contact area and encapsulating the semiconductor chip as taught by Galli et al for protecting the chip from being damaged.

As to claims 12 and 17, Shigeta et al discloses in figures 10E-10H a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method,

comprising: providing a leadframe (113/“patterns” 105) from a flexible multi-layered sheet (comprising layers 106 and 105) which has a first chip connection region (a first chip connection region is a connection region of first terminal 110 on lead 105) and a second chip connection region (a second chip connection region is a connection region of second terminal 110 on lead 105), the flexible multi-layered sheet that comprises a metal foil (comprising "patterns” 105) and a plastic film (106), the plastic film (106) being arranged on, and connected to, the metal foil (“patterns” 105), and having a plurality of openings (see figures 10E-10H, layer 106 having openings) in the regions arranged on the chip connection regions; providing a semiconductor chip (see the chip having terminals 110), which contains an active, and has a first contact area (first terminal 110) and a second contact area (second terminal 110); mounting the semiconductor chip (see the chip having terminals 110) in one of the plurality of openings of the plastic film (106) with the first contact area (first terminal 110) contacting the first chip connection region of the leadframe (113/"patterns” 105); connecting the second contact area (second terminal 110) to the second chip connection region of the leadframe (113/"patterns” 105).

Shigeta et al does not disclose the semiconductor chip contains radiation-emitting region and is encapsulated with a transparent or translucent encapsulating material; and wherein in the encapsulating step, a runner is led through a plurality of chips arranged on the multi-layered sheet.

Galli et al discloses in figure 6b an apparatus comprising a semiconductor chip (30) contains radiation-emitting region (“diode”, see col. 1, lines 19-26) and is encapsulated with a transparent or translucent encapsulating material (“plastic encapsulant” 45); and wherein in the

encapsulating step, a runner is led through a plurality of chips (84) arranged on the multi-layered sheet (comprising elements 60, 42) (see claims 9-12). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Shigeta et al by having a semiconductor chip that contains radiation-emitting region and is encapsulated with a transparent or translucent encapsulating material; and wherein in the encapsulating step, a runner is led through a plurality of chips arranged on the multi-layered sheet as taught by Galli et al for providing different application and protecting the chip from being damaged.

6. Claims 13-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta et al (U.S. 6,107,678) in view of Galli et al (U.S. 3,781,596) as applied to claim 12 above, and further in view of Jung et al (U.S. 4,812,421).

As to claims 13-14, Shigeta et al in view of Galli et al does not disclose the steps of providing a leadframe comprising punching the thin film metal foil in order to define the first and second connection regions, and punching the plastic film in order to define openings for the electrical connection of the semiconductor chip.

Jung et al discloses in figures 5-10 an apparatus comprising the steps of providing a leadframe (60, 42) comprising punching the thin film metal foil (42) in order to define the first and second connection regions, and punching the plastic film (60) in order to define openings (90) for the electrical connection of the semiconductor chip (see col. 5, lines 50-55). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Shigeta et al in view of Galli et al by having the steps of

providing a leadframe comprising punching the thin film metal foil and punching the plastic film as taught by Jung et al for electrically isolating the "beam leads"/(metal foil).

As to claim 15, Shigeta et al discloses in figures 10E-10H a surface-mountable miniature luminescent diode or photodiode with a chip package and a corresponding method, wherein the step of providing a leadframe (113/"patterns" 105) comprises the adhesive bonding of the foil ("patterns" 105) and the film (106).

As to claim 19, Shigeta et al in view of Galli et al does not disclose a plurality of chips arranged on the multi-layered sheet are tested for their functional capability after the encapsulating step and in that, for this purpose, the individual chips are electrically isolated when they are mounted.

Jung et al discloses in figures 5-10 an apparatus comprising a plurality of chips (84) arranged in the leadframe (comprising elements 42, 60) and wherein the individual chips (84) are electrically isolated when they are mounted. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Shigeta et al in view of Galli et al by providing a plurality of individual chips as taught by Jung et al for the purpose of producing/making a plurality of individual semiconductor devices/packages.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 3 and 6-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X Le, can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T. Y. T./

Examiner, Art Unit 2892

/Phuc T Dang/

Primary Examiner, Art Unit 2892